REMARKS

In response to the Final Office Action mailed February 1, 2008, Applicants respectfully request reconsideration and entry of this amendment. Claims 1 and 3-30 were previously pending in this application. By this amendment, claims 24 and 26-30 have been amended. As a result, claims 1 and 3-30 are pending for examination with claims 1, 24, 26 and 30 being independent. No new matter has been added.

Rejections under 35 U.S.C. §112

The Office Action rejected claims 26, 27 and 30 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

On page 2, the Office Action states that "the FIFO in the specification is located in the system, external to the stream register unit not in the stream register unit itself." The present specification supports both a FIFO coupled to a peripheral and a FIFO of the stream register unit. For example, on page 5, lines 14-15, the present specification states that [t]o improve the flow of data through the system, *the stream register unit 5 can also contain a small FIFO 17.* (Emphasis added). Therefore, the FIFO is not external to the stream register unit. This FIFO is shown in Figures 2a, 3 and 4 and is discussed throughout specification. For example, on page 7, the present specification describes that "If a data item requested by the execution unit 27 of the CPU 2 is not in the next location in the stream register FIFO17, the stream register 5 sends a stall signal to the execution unit 27 (arrow 46), thus causing the execution unit 27 to stall running of the program." Moreover, independent claims 1 and 24 also recite **both** a FIFO coupled to the peripheral and at least one stream register unit FIFO included in the stream register unit. (Emphasis added).

The Office Action indicates that "The Examiner will best interpret limitations outlining the stream engine to recite the alternative obvious variant of the enable instance where the FIFO is external to the stream register unit as seen in claims 1 and 11." Applicants respectfully note that claim 1 recites **two** types of FIFOs: "a FIFO coupled to the peripheral" and "at least one stream register unit FIFO." (Emphasis added). Indeed, claim 1 recites, inter alia,

> "a stream register unit being part of the processor and configured to supply a first type of data to the execution unit, the first type of data being data supplied

from a peripheral, the stream register unit including *at least one stream register unit FIFO* configured to store the first type of data received from the peripheral;

a FIFO coupled to the peripheral to receive said first type of data from the peripheral and connected to the stream register unit by a communication path, along which said first type of data can be supplied from the FIFO to the at least one stream register unit FIFO."

(Emphasis added)

Thus, claim 1 recites at least two types of FIFOs - at least one stream register unit FIFO and a FIFO coupled to the peripheral. The specification and the drawing support the two types of FIFOs shown by way of example as components 16 and 17, respectively. Independent claims 24 and 30 recite at least one FIFO *of the stream register unit.* (Emphasis added).

The Office Action states that the specification "at best hints at stream engine functionality." While Applicants respectfully disagree, claims 26-30 have been amended to further the prosecution of the present application.

Accordingly, withdrawal of this rejection is respectfully requested.

Rejections Under 35 U.S.C. §103

I. The Office Action rejected claims 1, 3-9 and 13-25 under 35 U.S.C. 103(a) as allegedly being unpatentable over Lewis et al. (U.S. Patent No. 5,797,043), hereinafter "Lewis," in view of George et al. (US Patent Number 6,785,829), hereinafter "George." Applicants respectfully disagree. Claim 24 has been amended to address a minor consistency issue and not for reasons related to patentability.

A. Independent Claim 1

Claim 1 recites:

A processing system for accessing data, the processing system comprising:

a processor comprising an execution unit for executing instructions;

a stream register unit being part of the processor and configured to supply a first type of data to the execution unit, the first type of data being data supplied from a peripheral, the stream register unit including at least one stream register unit FIFO configured to store the first type of data received from the peripheral;

a FIFO coupled to the peripheral to receive said first type of data from the peripheral and connected to the stream register unit by a communication path,

along which said first type of data can be supplied from the FIFO to the at least one stream register unit FIFO; and

a memory bus, separate from the communication path, connected between a data memory and the processor, across which the processor can access a second type of data, the second type of data being randomly accessible data held in the data memory;

wherein the first type of data is supplied via the communication path directly from the FIFO coupled to the peripheral to the stream register unit of the processor and the second type of data is supplied via the memory bus, separate from the communication path, between the data memory and the processor.

On page 4, the Office Action asserts that Lewis teaches some limitations of claim 1. Thus, the Office Action alleges that Lewis teaches a stream register unit being part of the processor and configured to supply a first type of data to the execution unit, the first type of data being data supplied from a peripheral (I/O Channel controller, element 62, figure 3, element 140, figure 5a), the stream register unit including at least one stream register unit FIFO configured to store the first type of data received from the peripheral (FIFO pool 172, figure 5a). Therefore, it appears that Office Action states that Lewis teaches the stream register unit as the I/O Channel controller. However, Lewis discusses a data transfer control system including a pool memory, a plurality of peripheral devices, and a transfer controller. (Lewis, col. 4, lines 22 -24). The pool memory provides for the storage of data in a plurality of FIFOs formed within the pool memory. (Lewis, col. 4, lines 24-26). The transfer controller is **coupled** to the pool memory and to the peripheral devices for selectively managing the transfer of data between the FIFOs and the peripheral devices. (Lewis, col. 4, lines 29-32). (Emphasis added). Thus, Lewis does not teach the stream register unit **including** at least one stream register unit **FIFO**, as recited in claim 1. (Emphasis added).

Moreover, on page 4, the Office Action states that Lewis teaches a FIFO coupled to the peripheral to receive said first type of data from the peripheral (column 14, lines 25-29). However, in this portion, Lewis again recites FIFO pool 172: "[t]he FIFO pool bus 144 is a dedicated bus for typically high-speed burst data transfers between the bus interface modules 148, 150, a FIFO pool 172 and any number of integrated peripherals and peripheral interfaces 174-188." (Lewis, col. 14, lines 25-29). Therefore, the Office Action refers to the FIFO pool of Lewis as teaching **both** a FIFO coupled to the peripheral and stream register unit FIFO recited in

claim 1. (Emphasis added). However, on page 2, the Office Action states that "the FIFO in the specification is located in the system, **external** to the stream register unit not in the stream register unit itself." (Emphasis added). This appears to contradict to the assertion that Lewis teaches both a FIFO coupled to the peripheral (which the Office Action asserts is external to the stream register unit) and a FIFO included in the stream register unit. Therefore, Lewis does not teach or suggest "a stream register unit being part of the processor and configured to supply a first type of data to the execution unit, the first type of data being data supplied from a peripheral, the stream register unit including at least one stream register unit FIFO configured to store the first type of data received from the peripheral; a FIFO coupled to the peripheral to receive said first type of data from the peripheral and connected to the stream register unit by a communication path, along which said first type of data can be supplied from the FIFO to the at least one stream register unit FIFO," as recited in claim 1.

Further, on page 5, the Office Action concedes that "Lewis fails to teach a system wherein a stream register unit being part of the processor." The Office Action then alleges that George "teaches, in an analogous system, a system wherein the stream register unit (cache, element 365, figure 3) forms part of the processor (processor, element 300, figure 3)."

Lewis states that the I/O channel controller core 26 that is part of the multi-function I/O peripheral controller hardware system 22 operates as a substantially autonomous bus master peripheral controller supporting multiple concurrent data and control signal transfers between the PCI bus 20 and system 22. (Lewis, col. 6, lines 38-42). George discusses that "[c]ache 365 is a special memory subsystem that stores frequently accessed data and its memory locations for **quick access by processor core** 363." (George, col. 5, lines 49-51). (Emphasis added). The Office Action states that it "would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis with the above teachings of George." However, it is not clear why one of ordinary skills in the art would combine Lewis and George. As discussed above, on page 4, the Office Action asserts that Lewis teaches a stream register unit as I/O Channel controller. However, the cache of George is a special memory subsystem.

The Office Action does not clearly indicate reasons for including, as asserted in the Office Action, the I/O channel controller of Lewis within a processor because a cache memory of George is included in a processor. For example, George discusses an I/O controller hub 210 that is a control circuitry associated an input or output devices that forms a hardware interface between the input/output devices and processor. (George, col. 3, lines 33-36).

Moreover, Lewis states that an "advantage of the present invention is that it **minimizes host processor performance loading** by performing **substantial autonomous** data transfer functions and dynamic flow management. The channel controller supports internal interrupt management that **minimizes both host and DSP interrupt support burdens**, thereby enabling and supporting real-time multiple parallel channel signal processing through a comprehensive interrupt source managed data stream channel connecting the host with auxiliary signal processing units." (Lewis, col. 4, lines 58-61). Thus, Lewis minimizes performance loading of the host processor. The Office Action states, somewhat ambiguously, that one of skill in the art would combine Lewis and George "in order to efficiently optimize a system with regards to real estate in compactness and means of high-speed processing." However, it appears that one of skill in the art would not be motivated to include the I/O channel controller of Lewis in the host processor for at least a reason that Lewis aims at minimizing host processor performance loading.

In view of the above, neither Lewis nor George teaches or suggests "a stream register unit being part of the processor and configured to supply a first type of data to the execution unit, the first type of data being data supplied from a peripheral, the stream register unit including at least one stream register unit FIFO configured to store the first type of data received from the peripheral; a FIFO coupled to the peripheral to receive said first type of data from the peripheral and connected to the stream register unit by a communication path, along which said first type of data can be supplied from the FIFO to the at least one stream register unit FIFO," as recited in claim 1.

In view of the foregoing, claim 1 patentably distinguishes over Lewis and George, either alone or in combination.

Claims 3-23 depend from claim 1 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 1 and 3-23 is respectfully requested.

B. Independent Claim 24

Claim 24, as amended, recites:

> A streaming data handling system, comprising:
> a processor comprising an execution unit for executing instructions;
> a stream register being part of the processor and configured to supply data from a peripheral to the processor, the stream register including at least one stream register FIFO configured to store the data received from the peripheral; and
> a FIFO memory coupled to the peripheral to receive the data from the peripheral and connected to the least one stream register FIFO via a communication path,
> wherein the stream register and the FIFO memory operate the same data handling protocol such that the stream register can receive streamed data items from the FIFO memory and supply them to the processor in the received order.

On pages 4 and 5, the Office Action rejected claim 24 for the same reasons as claim 1. The Office Action does not address the limitation of claim 24 that recites that "the stream register and the FIFO operate the same data handling protocol such that the stream register can receive streamed data items from the FIFO memory and supply them to the processor in the received order."

As discussed above, neither Lewis nor George teaches or suggests "a stream register being part of the processor and configured to supply data from a peripheral to the processor, the stream register including at least one stream register FIFO configured to store the data received from the peripheral; and a FIFO memory coupled to the peripheral to receive the data from the peripheral and connected to the least one stream register FIFO via a communication path," as recited in claim 24. Further, neither Lewis nor George teaches or suggests "the stream register and the FIFO operate the same data handling protocol such that the stream register can receive streamed data items from the FIFO memory and supply them to the processor in the received order," as recited in claim 24.

In view of the foregoing, claim 24 patentably distinguishes over Lewis and George, either alone or in combination.

Claim 25 depends from claim 24 and is allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 24 and 25 is respectfully requested.

II. The Office Action rejected claims 26-30 under 35 U.S.C. 103(a) as being unpatentable over Lewis in view of Garcia et al. (US Patent Number 6,433,785), hereinafter "Garcia."

C. Independent Claim 26

Claim 26 recites:

> A stream register being part of a processor comprising an execution unit, the stream register being connectable between the execution unit and a peripheral and comprising:
> a receiver arranged to receive a request for a data item from the execution unit; and
> at least one FIFO configured to store the data item received from the peripheral; wherein the stream register is arranged to:
> receive the request for the data item;
> determine whether the requested data item is in the at least one FIFO;
> if the requested data item is not in the at least one FIFO, send a stall signal to the execution unit of the processor; and
> send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item, and, if the data item is available, send the data item to the processor, and, if the data item is not available and if the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request.

On page 12, the Office Action states, "as per claims 26 and 30, Lewis teaches a stream register being part of a processor comprising an execution unit, the stream register being connectable between the execution unit and a peripheral." Applicants respectfully note that, on page 5, the Office Action concedes that Lewis **fails to teach a system wherein a stream register unit being part of the processor**. (Emphasis added). The Office Action noted that claims 26-30 are considered "as best interpreted in light of the 35 U.S.C. §112 rejection. However, the rejection does not seem to address the issue of the stream register being part of a

processor. Moreover, claim 26 has been amended to address the rejection under 35 U.S.C. §112. Therefore, Lewis does not teach limitations of claim 26.

Moreover, on page 12, the Office Action concedes that "Lewis fails to teach a register wherein if the data item being requested is not available, sending a timeout signal to the processor." The Office Action then alleges that Garcia teaches this limitation as timeout counter, column 5, lines 26-42. Garcia discusses that if the second transaction request is received while the posted write buffer 126 is unavailable, the timeout counter 124 is initiated. (Garcia, col. 4, lines 3-6). In one embodiment of Garcia, the timeout counter 124 counts six periods of a host bus clock before expiring. (Garcia, col. 4, lines 6-7). Other embodiments may use other clock signals as a reference, or may count different numbers of clock periods before expiring. (Garcia, col. 4, lines 7-9). As a result of the assertion of the second request pending signal 320 and the continued non-assertion of the posted write buffer available signal 350, the timeout counter 124 is initiated with a count of 6 at time C. (Garcia, Fig. 3; col. 5, lines 29-33). The timeout counter 124 begins counting down from time C until the posted write buffer available signal 350 is asserted at time D, indicating that the posted write buffer 126 is available to receive the data associated with the first postable write transaction request. (Garcia, Fig. 3; col. 5, lines 33-37).

Thus, the timeout **counter** of Garcia **counts down** until the posted write buffer becomes available for the second transaction. (Emphasis added). In contrast, claim 26 recites sending a timeout **signal** to the execution unit of the processor **causing the processor to interrupt** such that it can execute tasks other than the request. (Emphasis added). Therefore, the timeout counter of Garcia is different from timeout signal recited in claim 26. In view of the above, Garcia does not teach or suggest "...if the data item is not available and if the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request[,]" as recited in claim 26.

In view of the foregoing, claim 26 patentably distinguishes over Lewis and Garcia, either alone or in combination.

Claims 27-29 depend from claim 26 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 26-29 is respectfully requested.

D. Independent Claim 30

Claim 30 recites:

A stream register being part of a processor comprising an execution unit, the stream register being connectable between the execution unit and a memory, the stream register comprising:

a receiver arranged to receive a request for a data item from the execution unit of the processor;

at least one FIFO configured to store the data item received from a peripheral; and

a stream engine, arranged to:

receive the request for the data item;

determine whether the requested data item is in the at least one FIFO;

if the requested data item is not in the at least one FIFO, send a stall signal to the execution unit of the processor; and

send the request to the memory and receive one or more signals back from the memory indicating availability of the requested data item, and, if the data item is available, send the data item to the execution unit of the processor, and, if the data item is not available and if the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request.

The Office Action rejects claim 30 for the same reasons as claim 26. As discussed above, neither Lewis nor Garcia, teach or suggest limitations of claim 30.

In view of the foregoing, claim 30 patentably distinguishes over Lewis and Garcia, either alone or on combination.

Accordingly, withdrawal of the rejection of claim 30 is respectfully requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

By: _____

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